OIPE MAR 22 2007 PATENT & TRADEMARK OFFICE

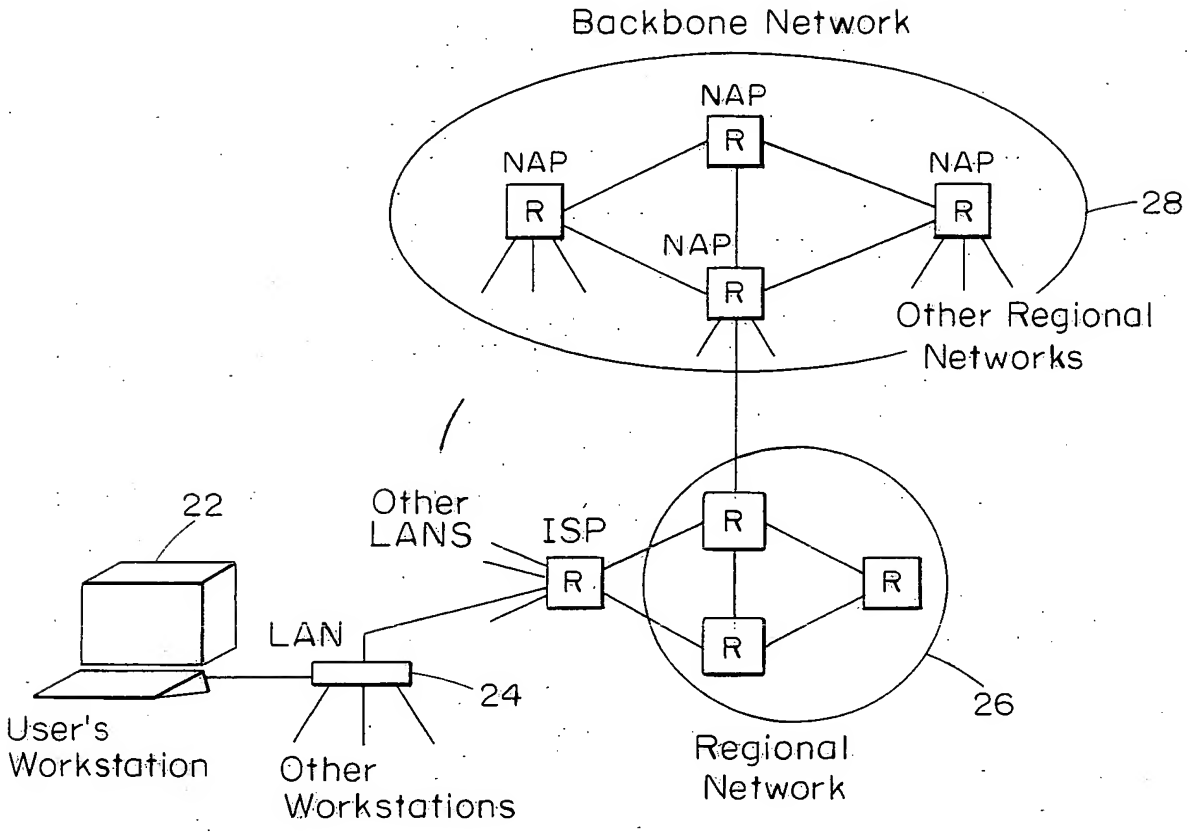

FIG. 1
PRIOR ART

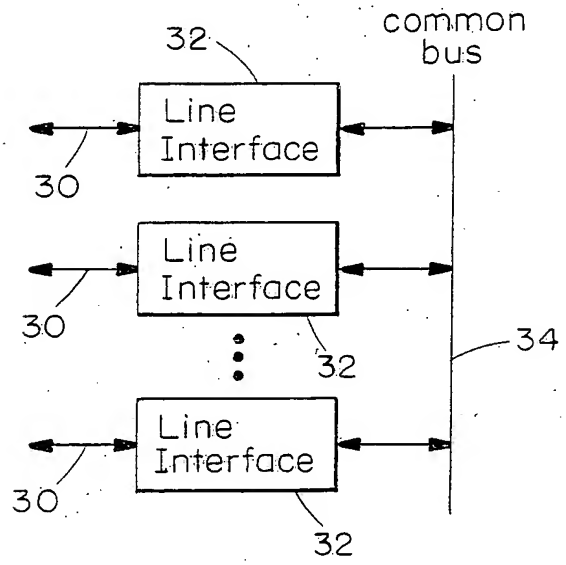

FIG. 2
PRIOR ART

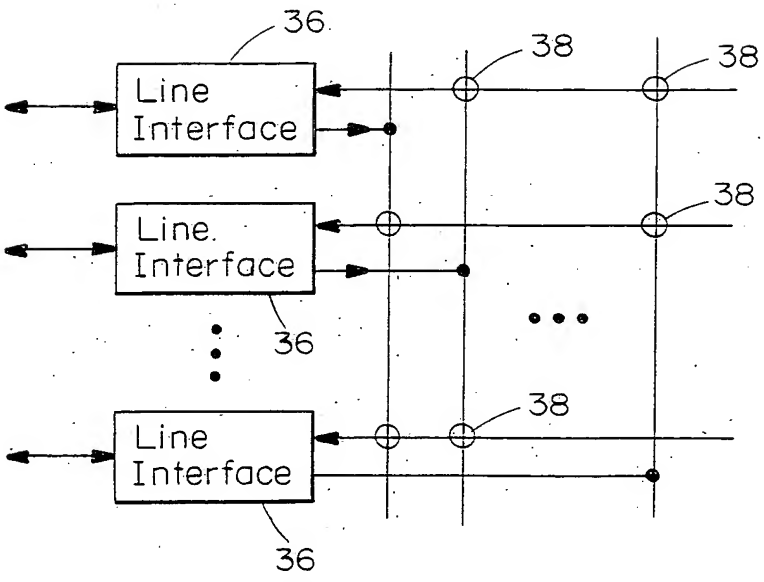

FIG. 3
PRIOR ART

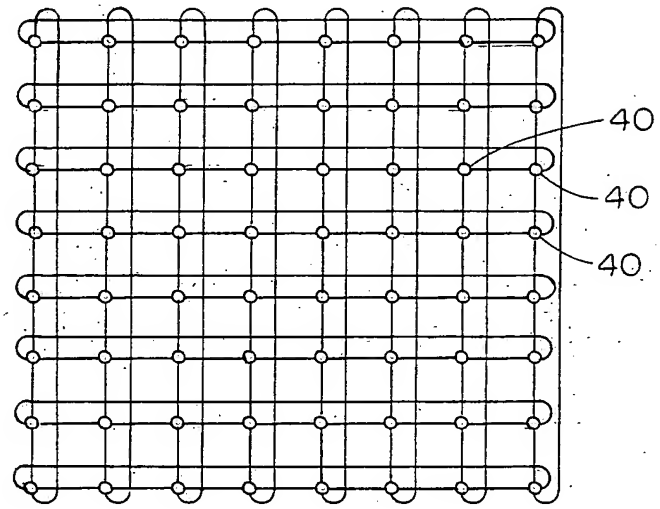

FIG. 4

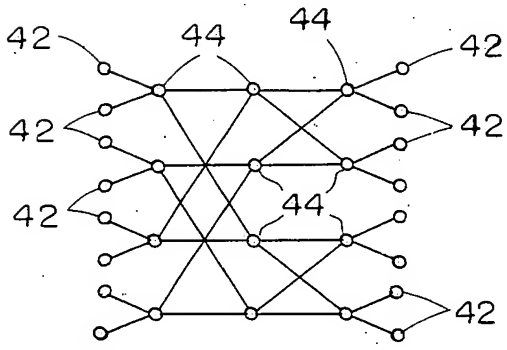

FIG. 5

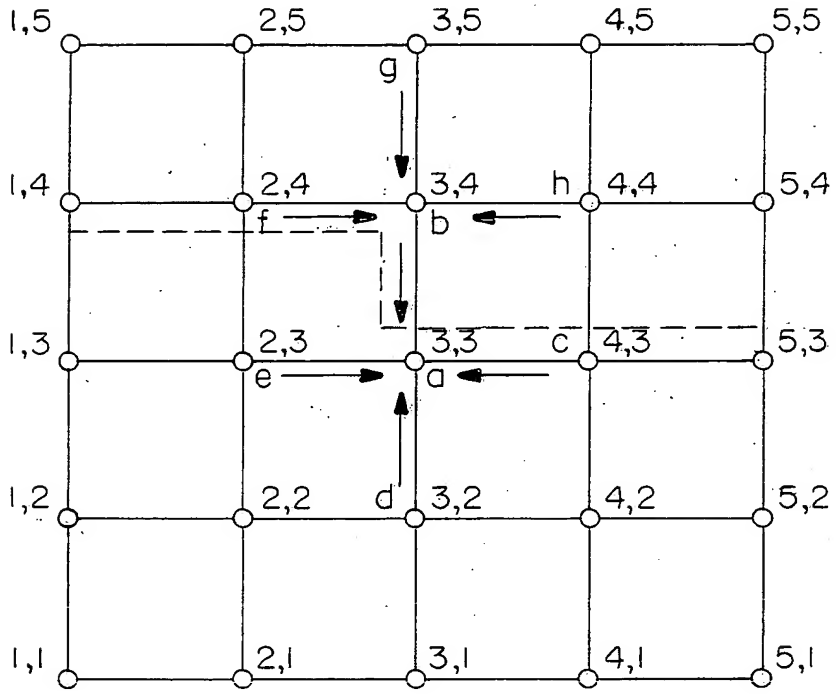
1,5
2,5
3,5
4,5
5,5
g
1,4
2,4
3,4
h
4,4
5,4
f
b
1,3
2,3
3,3
c
4,3
5,3
e
a
1,2
2,2
d
3,2
4,2
5,2
1,1
2,1
3,1
4,1
5,1

FIG. 6

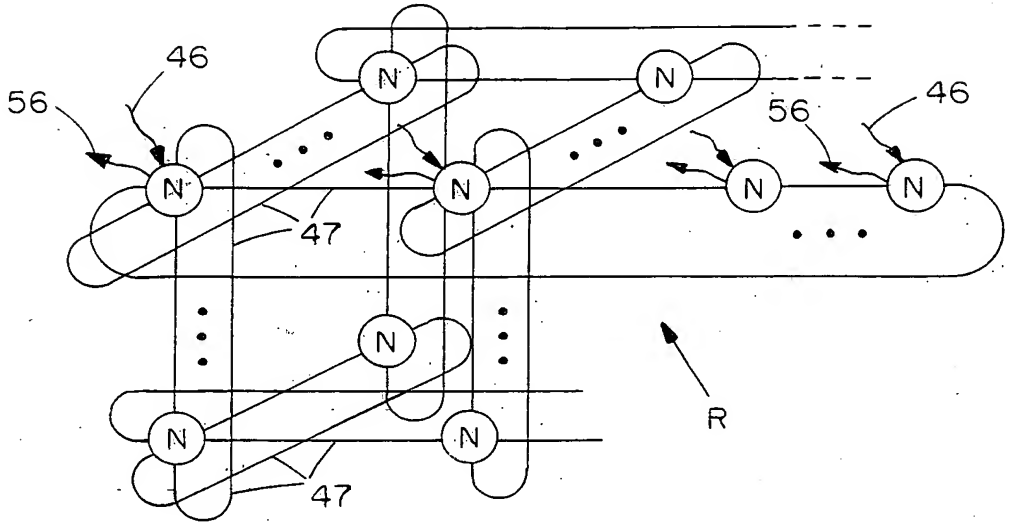
46
56
N
47
R

FIG. 7

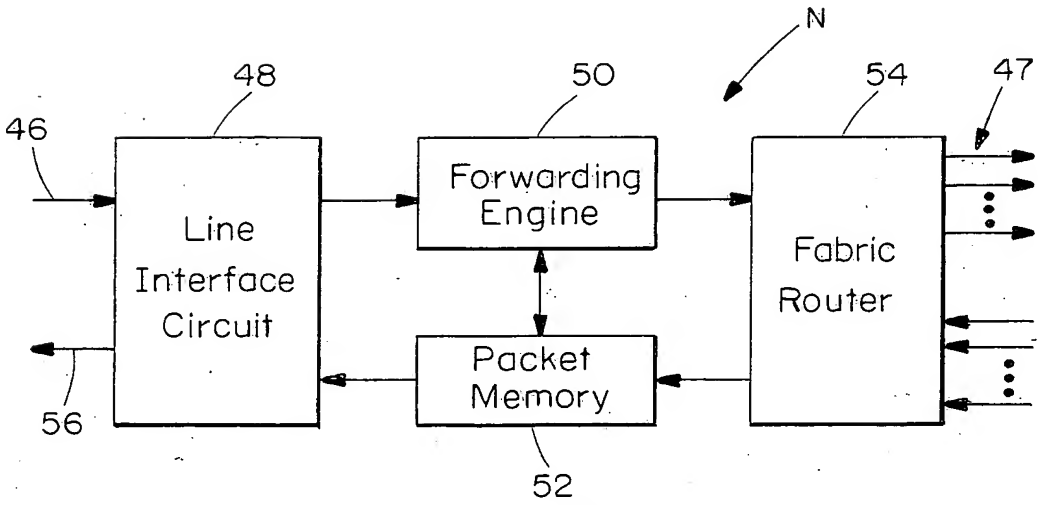
N
48
50
54
47
46
Line Interface Circuit
Forwarding Engine
Fabric Router
Packet Memory
56
52

FIG. 8

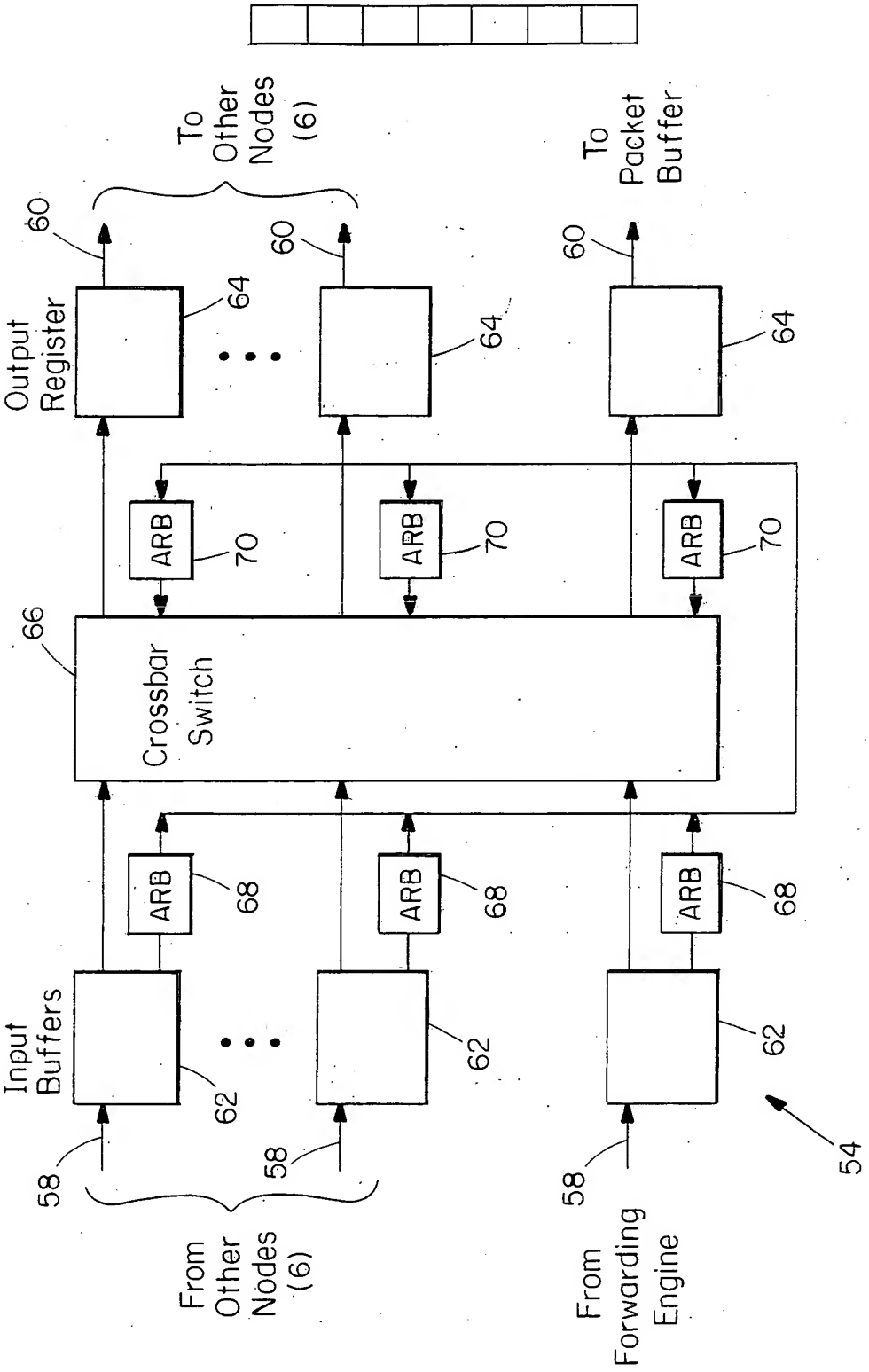
To Other Nodes (6)
To Packet Buffer
60
64
Output Register
ARB
70
66
Crossbar Switch
68
Input Buffers
62
58
From Other Nodes (6)
From Forwarding Engine
54

FIG. 9

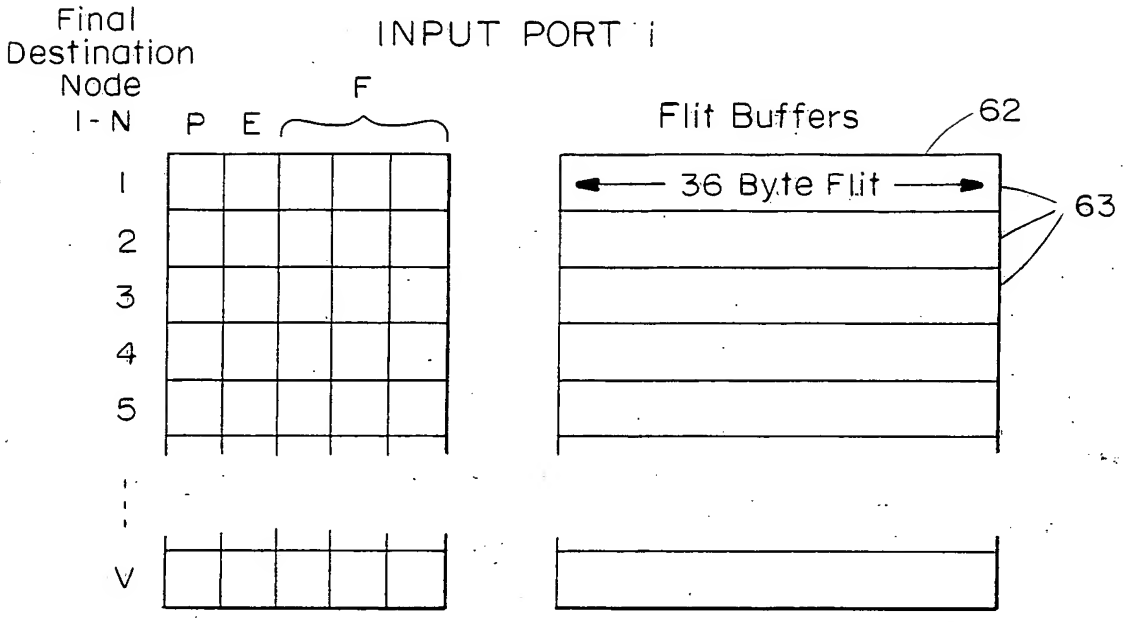

FIG. 10A

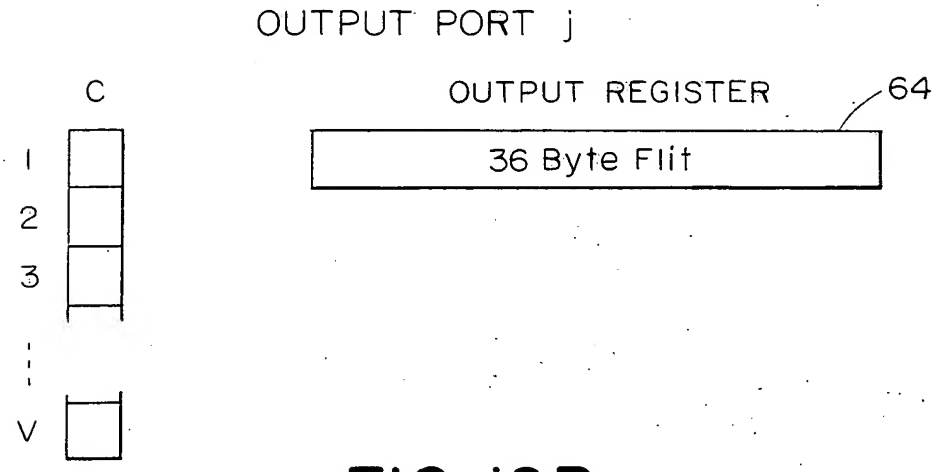

FIG. 10B

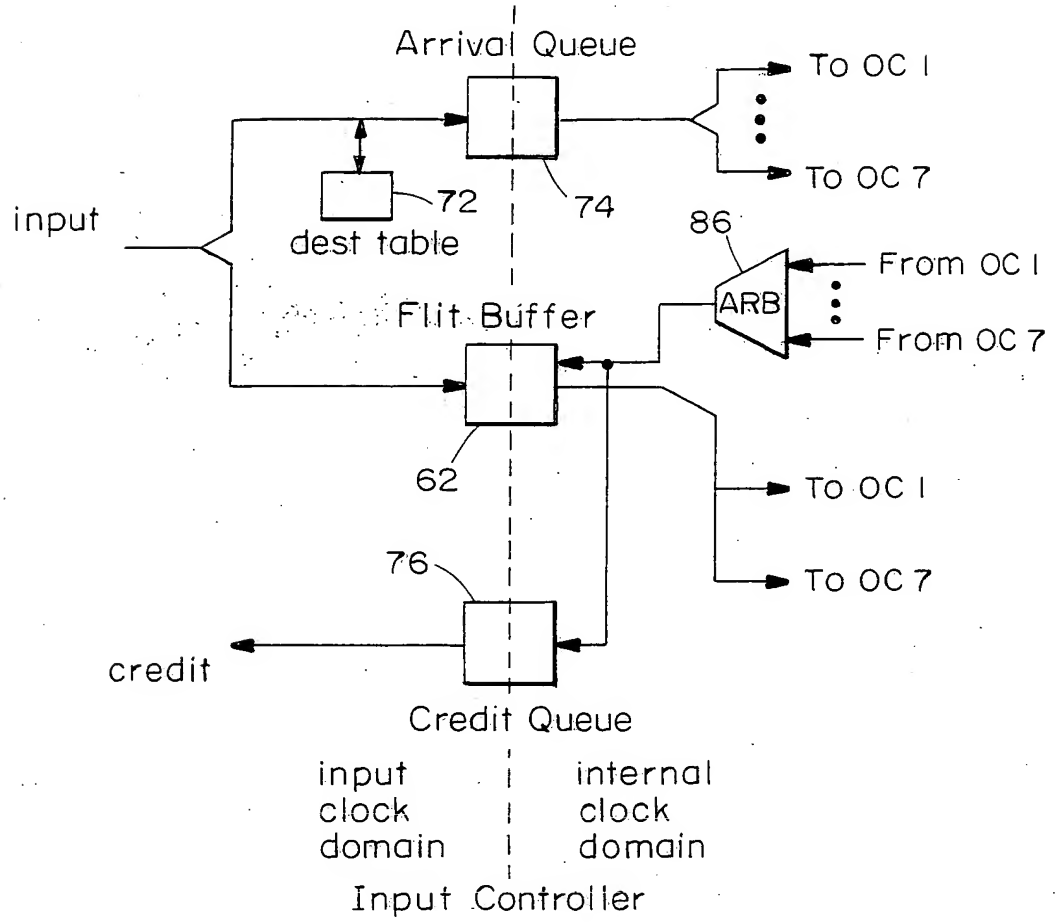

FIG. 11A

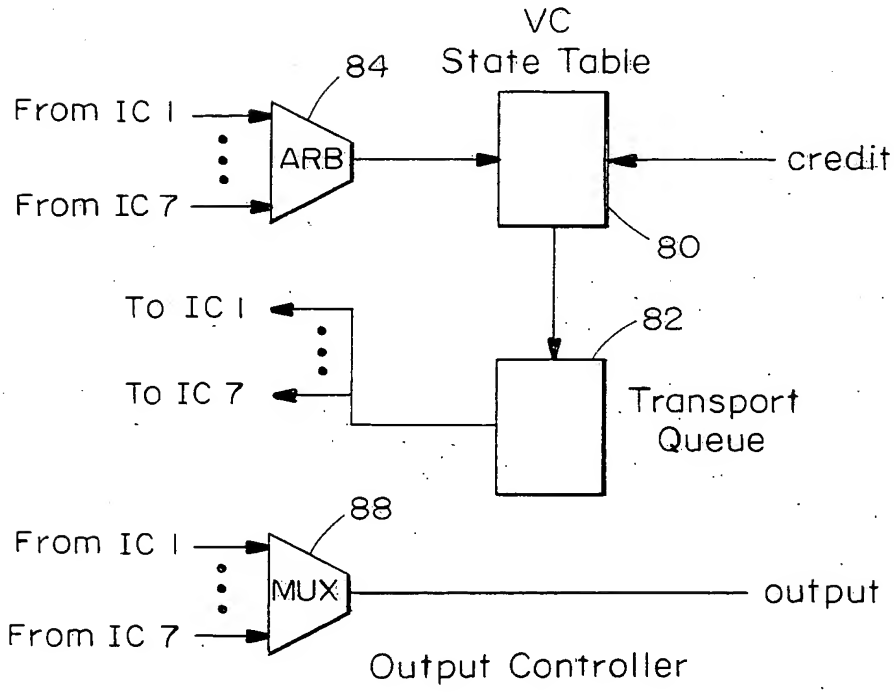

FIG. 11B

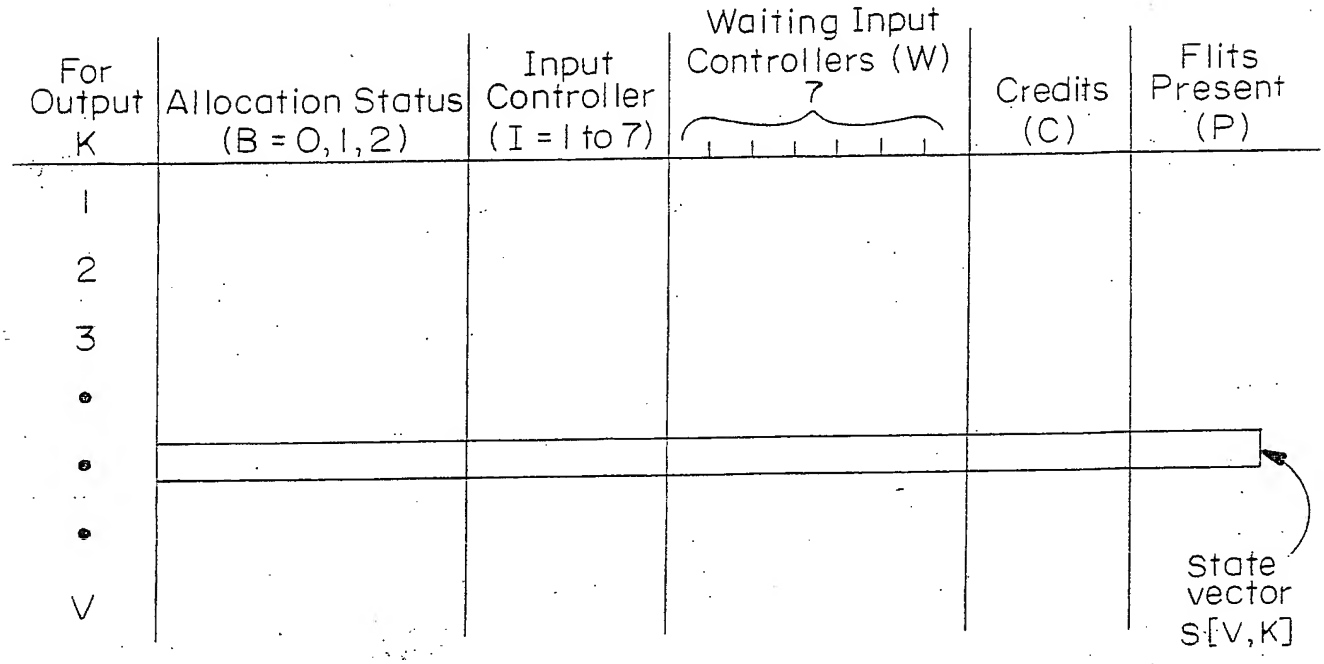
For Output K
Allocation Status (B = 0, 1, 2)
Input Controller (I = 1 to 7)
Waiting Input Controllers (W)
7
Credits (C)
Flits Present (P)
1
2
3
V
State vector s[V,K]

FIG. 12

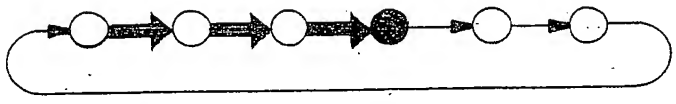

FIG. 13